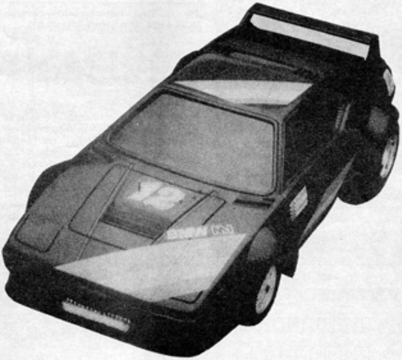
16-CHANNEL RUNNING LIGHT

W. Werner

This month we turn our attention to a less serious design. The robots in the popular TV series 'Battlestar Galactica', and the super-intelligent car 'Kitt' in 'Knight Rider' are credited with seeing abilities obtained from an electronic eye. The running lights circuit described here simulates such a scanning eye, and is aimed at our younger readers, the budding 'Knight-Riders' and model robot constructors.



The circuit diagram of Fig. 1 shows that the anodes of the 16 LEDs that simulate the scanning eye are commoned and connected to the +12 V supply via R_1. We can make any 1 of the 16 LEDs light by connecting its cathode to the negative supply rail, which is the same as ground in the present case. Circuit IC_3 is the electronic equivalent of a single-pole 16-way rotary switch because it takes the cathode connections to ground in a sequential manner. Only one LED lights at a time. First, output S0 goes low, then S1, then S2 and so on, to S15. Upon reaching S15, the 'switch' is turned back again to S14, S13, and so on, down to S0.

Each LED connected to IC_3 can be thought of as having a number between 0 and 15. This number is applied in binary coded decimal (BCD) form to inputs D1–D4 of IC_3. This should make the type description of the IC, *4-to-16 decoder*, clear: the device converts the 4-bit code applied to D1–D4 into the corresponding decimal number, 0 through 15. Since only one output is active (that is, logic low) at a time, the description *1-of-16 decoder* may also be used.

With 4 digital selection inputs, $2^4 = 16$ channels can be addressed individually. Output channel 0 (IC_3 terminal S0) is actuated by binary code 0000, and output channel 15 (IC_3 terminal S15) by binary code 1111. Table 1 lists all intermediate values, and shows the 'walking zero' in the output line configuration. Control input D1 changes state at the highest rate (0-1-0-1, etc.), and is therefore called the *least-significant* (LS) address line. Control input D4 changes state at every eighth transitions of D1. In the present 4-bit system, it is therefore the *most-significant* (MS) address line.

Counter and clock generator

The 1-of-16 decoder/LED driver is addressed by a counter, IC_2. This IC contains 4 series-connected bistables. Each of these divides its input frequency by 2, and supplies its output signal at a pin designated Q. Since there are 4 internal bistables, outputs QA through QD can take on 16 different logic configurations.

The clock signal applied to input CLK of IC_2 is divided by 2 in the first internal divider, which is associated with output QA. The clock signal divided by 4 appears on output QB, divided by 8 on QC, and divided by 16 on QD. This means that QA changes at the highest rate, so that it can be connected to input D1 of the LED decoder, IC_3. Similarly, MS output bit QD of the counter changes every 8 transitions of QA, so that it can be used for driving the MS address input of the LED decoder. The operation of the counter is illustrated by the timing diagram of Fig. 2.

Input $U/\overline{D}$ allows the counter chip to be programmed to count up (0 to 15; $U/\overline{D}$=1) and down (15 to 0; $U/\overline{D}$=0). The bistable built from NAND gates N_2 and N_3 ensures that the count direction is reversed automatically when state 0 or 15 is reached.

Pin 8 of gate N_3 functions as the SET input of the bistable, and pin 6 of N_2 as the RESET input. Pin 10 of N_3 forms output Q, and pin 4 of N_2 output $\overline{Q}$. The logic state of Q is always complementary to that of $\overline{Q}$. Output Q goes high when the bistable is set, and $\overline{Q}$ when the bistable is reset. In the present circuit, only output Q is used. A logic 0 at pin 8 of N_3 causes the bistable to be set, and output Q to go high. Output Q is made low again by a logic 0 at pin 6 of N_2.

The circuit diagram shows that the bistable is set and reset by the logic low levels supplied by LED decoder outputs S0 and S15 respectively. When S0 goes low (D_1 lights), it simultaneously causes the NAND bistable to be set, so that counter control input $U/\overline{D}$ is made high. As a result, the counter starts to count up from state 0. Similarly, when S15 goes low (LED D_{16} lights), $U/\overline{D}$ is pulled low, so that the count direction is reversed.

Inputs A through D of counter IC_2 are *jamming-inputs* that enable a preset value to be loaded when input PE (preset enable) is made logic high. Since the counter is to start at state 0000, all 4 jamming inputs have been tied to ground. Components C_2 and R_3 briefly take the PE input high at power-on, causing the counter to load '0000' as the preset value.

The $\overline{CI}$ (carry in/clock enable) of the counter is made permanently low to enable the counter to work continuously. Counting is halted, and the current output state is frozen if $\overline{CI}$ is taken high. This option is not required here, however.

Count mode input $B/\overline{D}$ (binary/decade) of IC_2 is connected to +12 V because binary counting is required.

The clock signal for the counter is provided by Schmitt-trigger NAND gate N_1 and frequency-determining components C_1-R_2. Together, these parts form an oscillator.

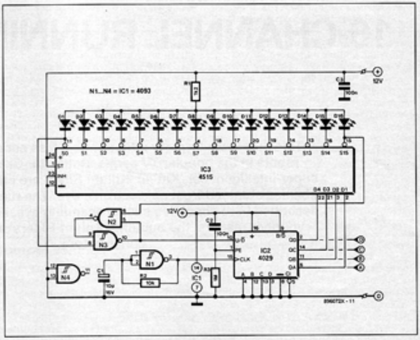


Fig. 1. The circuit is essentially composed of a 1-of-16 decoder/LED driver (IC3), a counter (IC2), and a clock generator (gate N1).

Construction

The present circuit is probably too com-

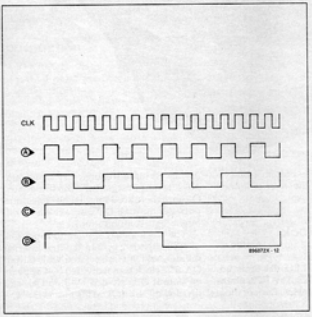


Fig. 2. Timing diagram illustrating the operation of counter IC2, which is composed of four cascaded bistables.

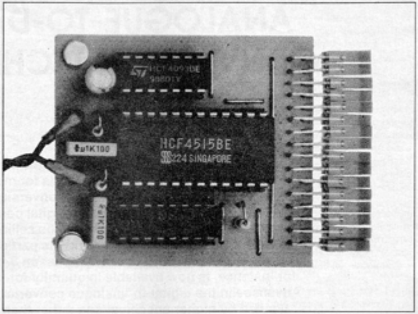
decimal	binary	1-of-16 code
	D4–D1	S0 S15
0	0000	0111111111111111
1	0001	1011111111111111
2	0010	1101111111111111
3	0011	1110111111111111
4	0100	1111011111111111
5	0101	1111101111111111
6	0110	1111110111111111
7	0111	1111111011111111
8	1000	1111111101111111
9	1001	1111111110111111
10	1010	1111111111011111
11	1011	1111111111101111
12	1100	1111111111110111
13	1101	1111111111111011
14	1110	1111111111111101
15	1111	1111111111111110

Table 1. Relation between the binary input and 1-of-16 decoded output of decoder IC3. Note the 'walking zero' in the output states.

plex to build on a Universal Prototyping Board as used for other projects in this series. The lay-out of a suitable printed-circuit board is, therefore, given in Fig. 3.

Refer to the Parts List when selecting the components. First mount the wire links, then the resistors, capacitors and IC sockets. The LEDs are fitted last. The introductory photograph illustrates the use of 16 rectangular LEDs whose terminals have been bent at right angles. Round LEDs are, of course, also suitable, and the constructor is left free to decide on the most realistic appearance of the electronic eye. Use a transparent red bezel in front of the LEDs to improve the visibility.

Although the supply voltage of the running lights is given as 12 V, the circuit also works fine when powered from a 9 V or 5 V source. Some experimenting with the value of R_1 and/or C_1 may be required, however, to obtain the desired scanning rate at relatively low supply voltages. Also, as a general rule, make R_1 smaller with low supply voltages to ensure sufficient LED brightness.



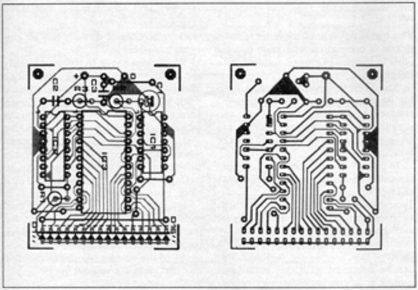


Fig. 3. Printed-circuit board for the running-lights circuit.

Parts list

Resistors:
R_1 = 1k2
R_2 = 10k
R_3 = 1M0

Capacitors:
C_1 = 10µ; 16 V; radial
C_2;C_3 = 100n

Semiconductors:
D_1 – D_{16} = LED; red; rectangular
IC_1 = 4093
IC_2 = 4029
IC_3 = 4515

Miscellaneous:
PCB 896072